

REMARKS / ARGUMENTS

Claims 1-4 and 6-10 are pending in this application. By this Amendment, Applicants amend Claims 1, 6, and 7.

Claims 1-4 and 6-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshihara et al. (U.S. 5,898,909). Applicants respectfully traverse the rejection of Claims 1-4 and 6-10.

Claim 1 has been amended to recite:

An RF module comprising;
a multi-layered substrate having a first major surface, a second major surface opposed to the first major surface, and side surfaces extending the between first and second major surfaces;
a base-band IC, a memory IC and an RF-IC, said base-band IC and memory IC being mounted on the first major surface of said multi-layered substrate, and said RF-IC being mounted on the second major surface of said multi-layered substrate;
an RF passive component incorporated in said multi-layered substrate;
a wiring pattern incorporated in said multi-layered substrate, said wiring pattern interconnecting said base-band IC and said memory IC; and
a shielding ground electrode pattern interposed between the first major surface of said multi-layered substrate on which said base-band IC and said memory IC are mounted and the second major surface of said multi-layered substrate on which said RF-IC is mounted. (Emphasis added.)

The Examiner alleged that Yoshihara et al. teaches all of the features recited in Applicants' Claim 1, including a base-band IC 11a and a memory IC 11c mounted on a first side of the multi-layered substrate 14, and an RF-IC 11b mounted on a second side of the multi-layered substrate 14.

Applicants' Claim 1 has been amended to recite the features of "a multi-layered substrate having a first major surface, a second major surface opposed to the first major surface, and side surfaces extending the between first and second major surfaces" and "a base-band IC, a memory IC and an RF-IC, said base-band IC and memory IC being mounted on the first major surface of said multi-layered substrate, and said RF-IC being mounted on the second major surface of said multi-layered substrate." Support for

these features is found, for example, in the paragraph bridging pages 2 and 3 and Fig. 1 of the originally filed application.

In contrast to Applicants' Claim 1, as clearly seen in Fig. 18 of Yoshihara et al. all of the elements 11a-11c, which the Examiner alleged correspond to a base-band IC, an RF-IC, and a memory IC, respectively, are disposed on the same (first) major surface of the substrate 14, and none of these elements are disposed on a second major surface of the substrate 14. In fact, Yoshihara et al. fails to teach or suggest that any elements could or should be disposed on the second major surface of the substrate 14. Thus, Yoshihara et al. certainly fails to teach or suggest the features of "a multi-layered substrate having a first major surface, a second major surface opposed to the first major surface, and side surfaces extending the between first and second major surfaces" and "a base-band IC, a memory IC and an RF-IC, said base-band IC and memory IC being mounted on the first major surface of said multi-layered substrate, and said RF-IC being mounted on the second major surface of said multi-layered substrate" as recited in Applicants' Claim 1.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 1 under 35 U.S.C. § 102(b) as being unpatentable over Yoshihara et al.

In view of the foregoing amendments and remarks, Applicants respectfully submit that Claim 1 is allowable. Claims 2-4 and 6-10 depend upon Claim 1, and are therefore allowable for at least the reasons Claim 1 is allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

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To the extent necessary, Applicants petition the Commissioner for a Three-Month Extension of Time, extending to December 15, 2006, the period for response to the Office Action dated June 15, 2006.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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/Christopher A. Bennett #46,710/
Attorneys for Applicant(s)

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT, LLP
8180 Greensboro Drive, Suite 850
Tyson's Corner, VA 22102
Telephone: (703) 637-1480
Facsimile: (703) 637-1499